AL502
Service Guide

15-inch LCD Monitor

1. Audio circuit (Circuit diagrams Main PWB)

1.1 Audio input

The audio signal input received from the audio input terminal (JK011) is applied to the amplifier I001 of 4 (L-CH) and 9 (R-CH) through the low-pass filter consisting of R040, R041, R042, R043, C040 and C041.

In this amplifier, controls of Volume and mute are conducted. The audio signal controlled at the pin 6 determines the attenuation of output of the amplifiers. Since then, the signal is output to the jack P003.

1.2 Audio output

The audio signal is output from P002 output terminal of the Audio block to the internal speaker system.

2. Power supply (Circuit daigrams MAIN PWB)

2.1 Line filter consists of C801, T801, C802, C803, C804. It eliminates high frequency interference to meet EMI's requirement.

2.2 Rec & Filter :

Bridge diode D801 converts AC source into pulsed DC. This pulsed DC is smoothed and filtered by C805.

R802 is an NTC (negative thermal coefficient) resistor, used to reduce inrush current to be within safe range.

2.3 Power transformer :

T802 converts energy for square wave from power source C805 to secondary side to generate +12V and +5V.

2.4 Output :

The square wave from T802 is rectified by D809, D810, then filtered by C817, C822 to generate +12V and +5V respectively.

2.4.1 A 5V power supply for LCD module, CPU and logic is generated from the power source.

2.4.2 I308 : 3-terminal regulator

A 3.3V power supply for I306 analog is generated from the 5V source.

2.4.3 I308 : 3-terminal regulator

A 3.3V power supply for I306 digital is generated from the 5V source.

Q302, Q303 ON/OFF control for LCD Module

ON/OFF control is performed for power ON/OFF and also for the power saving sequence.

2.5 Driver :

Q803 drive T802 from PWM control of I801 for power converted.

2.6 FB :

Negative feedback CKT consists of photo coupler I802 and adjustable regulator I803. It can maintain output voltages +5V and +12V at a stable level.

2.7 PWM :

2.7.1 *Start* : When power is turned on, Q801 conducts due to bias from C805 and R805,R803. C807 is charged a 16 volt and a starting current about 0.3mA to pin 7 of I801. I801 starts to oscillate and outputs a pulse train through pin 6 to drive Q803.

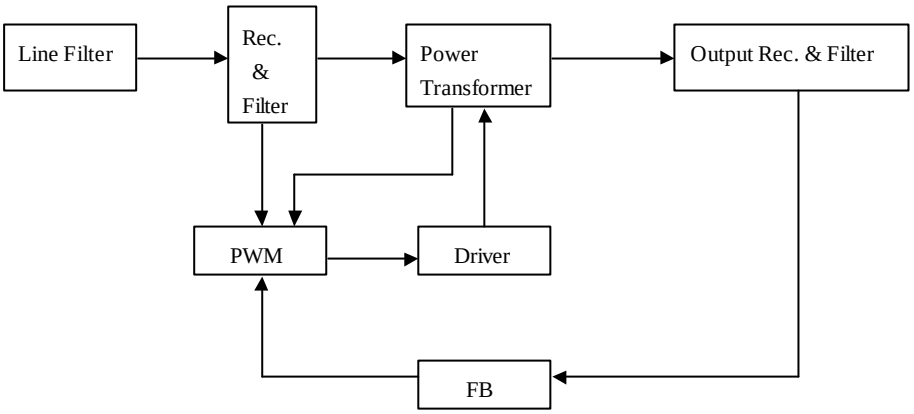
2.7.2 *OPP* : When Q803 turns on, C805 supplies a linearly increasing triangle current through the primary induc tance of T802 to the driver Q803, once the peak value of this current multiplied by R811 exceeds 1 volt, pulse train will be shut down immediately to protect Q803, T802 from being burned out.

2.7.3 *Regulation* : If output voltage +5V goes up, the R terminal of I803 gets more bias, accordingly photo transis tor and photo diode flows more current. The voltage of pin 2 goes up too, making the pulse width of pin 6 to become narrower. So the output voltage +5V will be pulled down to a stable value.

2.7.4 *OVP* : If +5V goes up too much, the induced voltage on pin 4 of T802 becomes large also. Suppose that it is over 18 volts, ZD801 conducts, pin 3 of I801 is pulled up over 1 volt. The pulse train at pin 6 goes down to zero, shutting Q803 off immediately.

2.7.5 *SCP* : If output terminal is short to ground, photo transistor does not conduct, hence Q806 does not conduct either. Then oscillation of I801 is stop, shutting Q803 off immediately.

H15AAU / H15AAR Power Board Block Diagram



3. On-screen circuit (Circuit diagrams Main PWB)

I300 Embeded function.

On-screen menu screen is established and the resultant data are output from I300 (Circuit diagram MAIN PWB).

4. Video input circuit (Circuit diagram MAIN PWB)

The AC-coupled video signal is used to clamp the black level at 0V).

5. Definition converter LSI peripheral circuit (Circuit diagram MAIN PWB)

I301 MRT V2 gmZAN1 is the definition A/D converter LSI.

The analog R, G, B signal input entered from the video input circuit is converted into the digital data of video signal through the incorporated A/D converter. Based on this conversion, this device performs interpolation during pixel extension. The source voltage for this device is 3.3V and the system clock frequency is 12MHz. The withstand voltage level for the input signal voltage is 3.3V and 5V.

6. System reset, LED control circuit (Circuit diagram MAIN PWB)

6.1 System reset

System reset is performed by detecting the rising and falling of the 5V source voltage at I302.

6.2 LED control circuit

Green / amber is lit with the control signal of the LED GREEN and LED AMBER signal pin 43, 42 from I303 (Circuit diagram MAIN PWB).

7. E^2PROM for PnP (Circuit diagram MAIN PWB)

8. E²PROM (Circuit diagram MAIN PWB)

Data transfer between I304 and CPU (Circuit diagram MAIN PWB page 4/7 (I303) is effected through the IIC bus SCL (pin 9) and SDA (pin 8) of I300 or SCL (pin 42) and SDA pin 39 of I301. The data to be transferred to each device are stored in I304.

- I300 control data.
- OSD related setting data.
- Other control data for service menu.

9. CPU circuit (Circuit diagram MAIN PWB)

I303 (MTV312M64) (SM89516C25) or (W78E62BP-40) functions as the CPU.

The source voltage for the device is 5.0V and the system clock frequency is 12MHz.

9.1 Detection of POWER switch status

The CPU identifies the ON status of the two power supplies. The identification is made when the power supply is turned off. For example, if the power supply is turned off with the POWER switch, the POWER switch must be turned on when activating the power supply again. If the power supply is turned off by pulling out the power cord, then this power supply can be turned on by connecting the power cord, without pressing the POWER switch.

9.2 Display mode identification

9.2.1 Functions

(1) Display mode identification

- The display mode of input signal is identified based on Table 1, and according to the frequency and polarity (HPOL, VPOL) of horizontal or vertical sync signal, presence of the horizontal or vertical sync signal, and the discrimination signal (HSYNC_DETECT, VSYNC_DETECT).
- When the mode has been identified through the measurement of horizontal and vertical frequencies, the total number of lines is determined with a formula of " Horizontal frequency / Vertical frequency = Total number of lines. "Final identification can be made by examining the coincidence of the obtained figure with the number of lines for the mode identified from the frequency.
- When the detected frequency if the sync signal has changed, the total number of lines should be counted even through it is rge identified frequency in the same mode. Then, it is necessary to examine whether the preset value for the vertical display position of Item 4-3 has exceeded the total number of lines. If exceeded, a maximum value should be set up, which does not exceed the vertical display position of Item 4-3.

(2) Out-of -range

This out-of-range mode is assumed when the frequency of the horizontal / vertical signal is as specified below.

- Vertical frequency : Below 50Hz or above 85Hz
- Horizontal frequency : Below 24 KHz or above 75 KHz

(3) Power save mode

The power save mode is assumed when the horizontal / vertical signals are as specified below.

- If there is no horizontal sync signal input.
- If there is no vertical sync signal input.
- If the horizontal sync signal is outside the measuring range of I300.
- If the vertical sync signal is outside the measuring range of I300.

Table 1

Mode	No	Resolution	H-freq (KHz)	Band Width (MHz)	Polarity	
					H	V
1.	247	VGA 720 x 350 70Hz	31.47	28.322	+	-
2.	102	VGA 720 x 400 70Hz	31.47	28.322	-	+
3.	103	VGA 640 x 480 60Hz	31.47	25.175	-	-
4.	182	MAC 640 x 480 66Hz	35	32.24	-	-
5.	173	VESA 640 X 480 72Hz	37.86	31.5	-	-
6.	109	VESA 640 X 480 75Hz	37.5	31.5	-	-
7.	104	VESA 800 x 600 56Hz	35.16	36	+	+
8.	116	VESA 800 x 600 60Hz	37.88	40	+	+
9.	110	VESA 800 x 600 75Hz	46.88	49.5	+	+
10.	117	VESA 800 x 600 72Hz	48.08	50	+	+
11.	108	MAC 832 x 624 75Hz	49.72	57.283	-	-
12.	118	VESA 1024 x 768 60Hz	48.36	65	-	-
13.	217	SUN 1024 x 768 65Hz	52.45	70.49	-	-
14.	157	VESA 1024 x 768 70Hz	56.48	75	-	-
15.	141	VESA 1024 x 768 75Hz	60.02	78.75	+	+

Attention :

1. When resolution beyond 1024 x 768 is inputted, resolution is lowered with Down scaling to 1024 x 768, and indicated, and OSD should indicate OUT of Range.

9.3 User Control

9.3.1 Related ports of I303

Port	Pin No.	I/O	Signal name	Function	Remarks
P1.5	7	I	POWER	Power switch input	Power ON , OFF control
P1.1	3	I	DOWN	▼ switch input	(▼) key
P1.0	2	I	UP	▲ switch input	(▲) key
P1.3	5	I	-	- switch input	(-) key
P1.2	4	I	+	+ switch input	(+) key

9.3.2 Functions

Control is effected for the push-switches to be used when the user changes the parameters, in order to modify the respective setting values. Whether the switch has been pressed is identified with the switch input level that is turned “L”.

Each switch input port is pulled up at outside of ASIC.

Each parameter is stored in the EEPROM, the contents of which are updated as required.

9.4 Control of definition converter LSI I300.

9.4.1 Ports related to control

Pin No.	I/O	Signal name	Function
159	I	IRQ	interrupt signal
5	I/O	SCL	serial clock
6	I/O	SDA	serial data

9.4.2 Functions

Major function of I300 are as follows:

(1) Expansion of the display screen.

(2) Timing control for various signal types.

(3) Power-supply sequence (LCD panel).

9.5 I^2C bus control

9.5.1 Related ports of I303

Port	Pin No.	I/O	Signal name	Function
P1.7	14	O	SCL	IIC bus clock
P1.6	13	I/O	SDA	IIC bus data

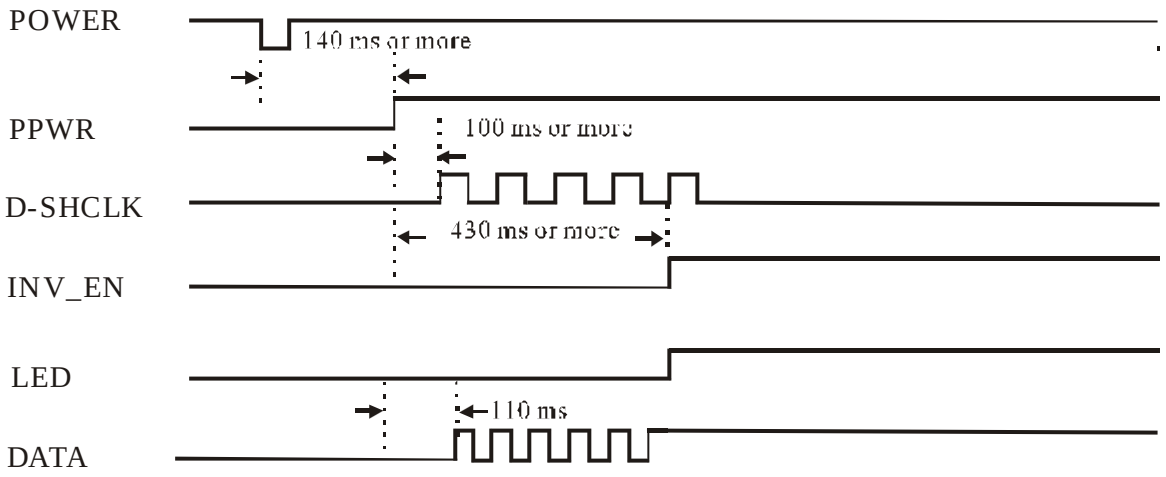
9.5.2 I^2C-controlled functions

The following functional controls are effected by I^2C.

(1) Control of EEPROM I304 for parameter setting.

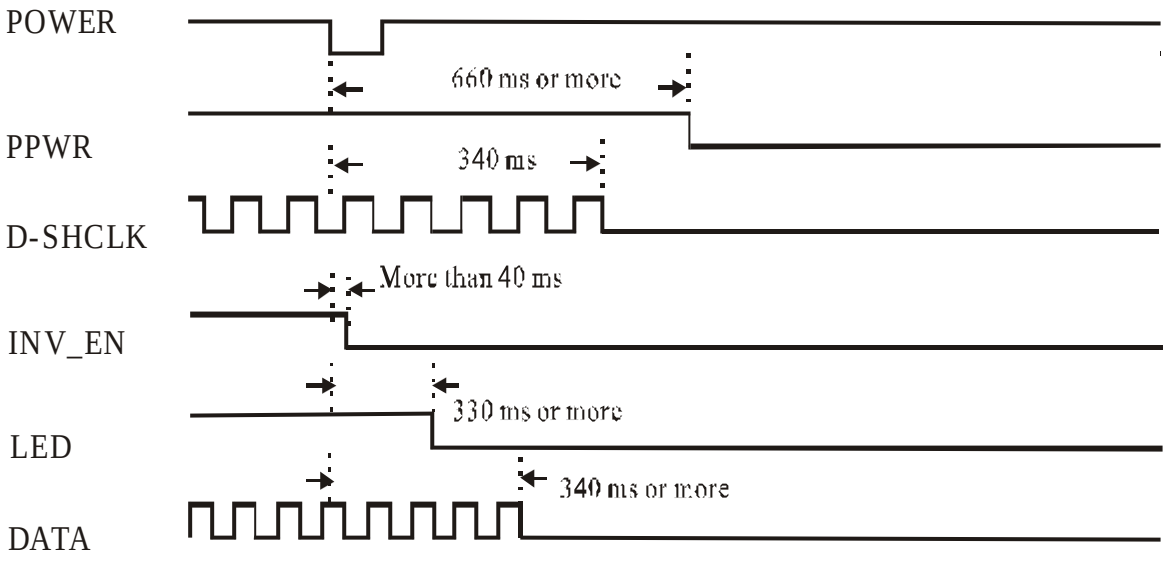
9.6 Power ON sequence

When the POWER switch is pressed, the POWER OFF signal is turned “H”. When this “H” potential is detected, the CPU begins to establish the respective power supplies according to the sequence shown below.



9.7 Power OFF sequence

When the POWER switch is pressed while the power supply is ON, the POWER ON signal is turned “H”. When tshown below.his “H” potential is detected, the CPU begins to turn off the respective power supplies according to thesequence



10. Inverter

This unit operates on an output voltage of 15V from power source.

10.1 Regulator: Q101 get a +5VDC for I102 power supply.

10.2 UVP: Q106 turns off when the Vin is under 14V. Then pin 3 of I102 is pulled low and inverter off immediately. That is the under voltage protection.

10.3 Control IC: I102 (OZ960S)

10.3.1 Enable : When pin 3 of I102 is over 1.5V, I102 works. If it is under 1.5V, I102 turns off.

10.3.2 OSC: When I102 enabled, R108/C115 (pin 17/pin18 of I102) determine the operating frequency.

10.3.3 SST: C104 (pin 4 of I102) provides soft start function.

10.3.4 Ignition: R109 (pin 8 of I102) provides higher operating frequency for more striking voltage until regulation of feedback of lamp current. C103 (pin 1 of I102) determine the striking time.

10.3.5 Dimming control: The divided voltage of R106/R105/R104 control the duty pulse of burst-mode to drive Q105 and perform a wide dimming control for the CCFL. The burst-mode frequency is determined by C116.

10.3.6 Regulation: Pin 9/pin 10 of I102 provide regulation of the CCFL current from feedback. The non-inverting reference (pin 10 of I102) is at 1.25V nominal.

10.3.7 Protection: Open-lamp protection in the ignition period is provided through both pin1 and pin 2 of I102. Removal of the CCFL during normal operation will trigger Q104 to turns on and shuts off the inverter. This is latch function.

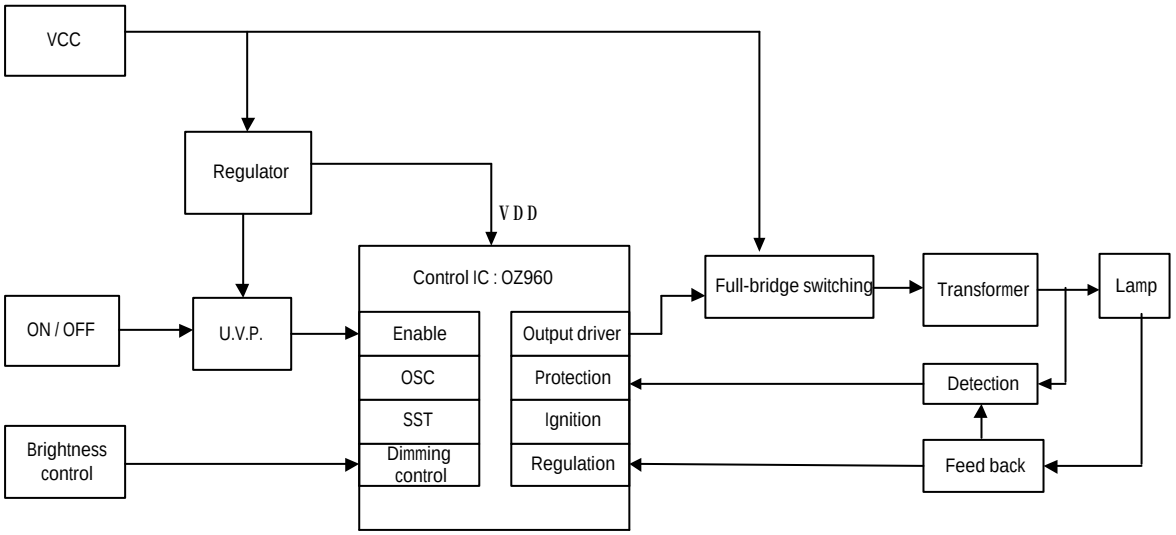
10.3.8 Output drivers: The configuration prevents any shoot-through issue associated with bridge-type power conversion applications. Adjusting the overlap conduction between I101 P-MOSFET and I103 N-MOSFET, I101 N-MOSFET and I103 P-MOSFET, the CCFL current regulation is achieved.

10.4 Full-bridge switching/Transformer: I101/I103 /C123/C125/T101/T102 compose full-bridge switching to convert DC into AC for driver the CCFL.

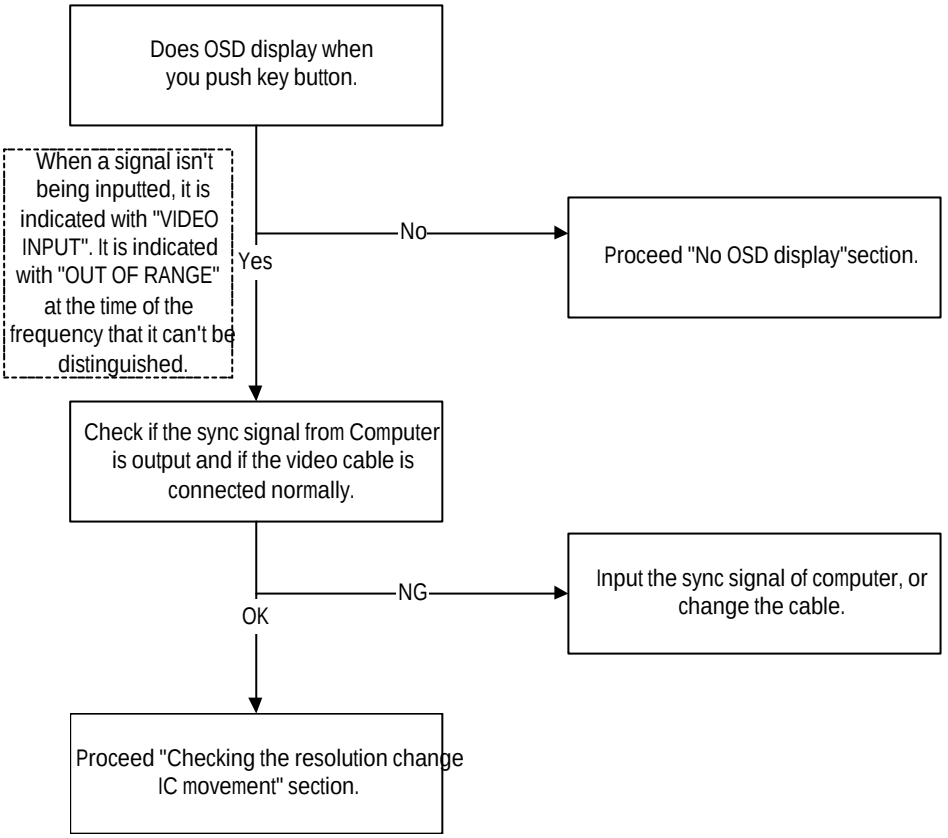
10.5 Detection: C124/C119/CR102 detect the output voltage and ensure a rated voltage by pin2 of I102. Q102/Q103 ensure not a open-lamp.

10.6 Feedback: CR101/R120/R121/D108 sense the lamp current for negative feedback and regulation. The divided voltage on R121 will be at 1.25V.

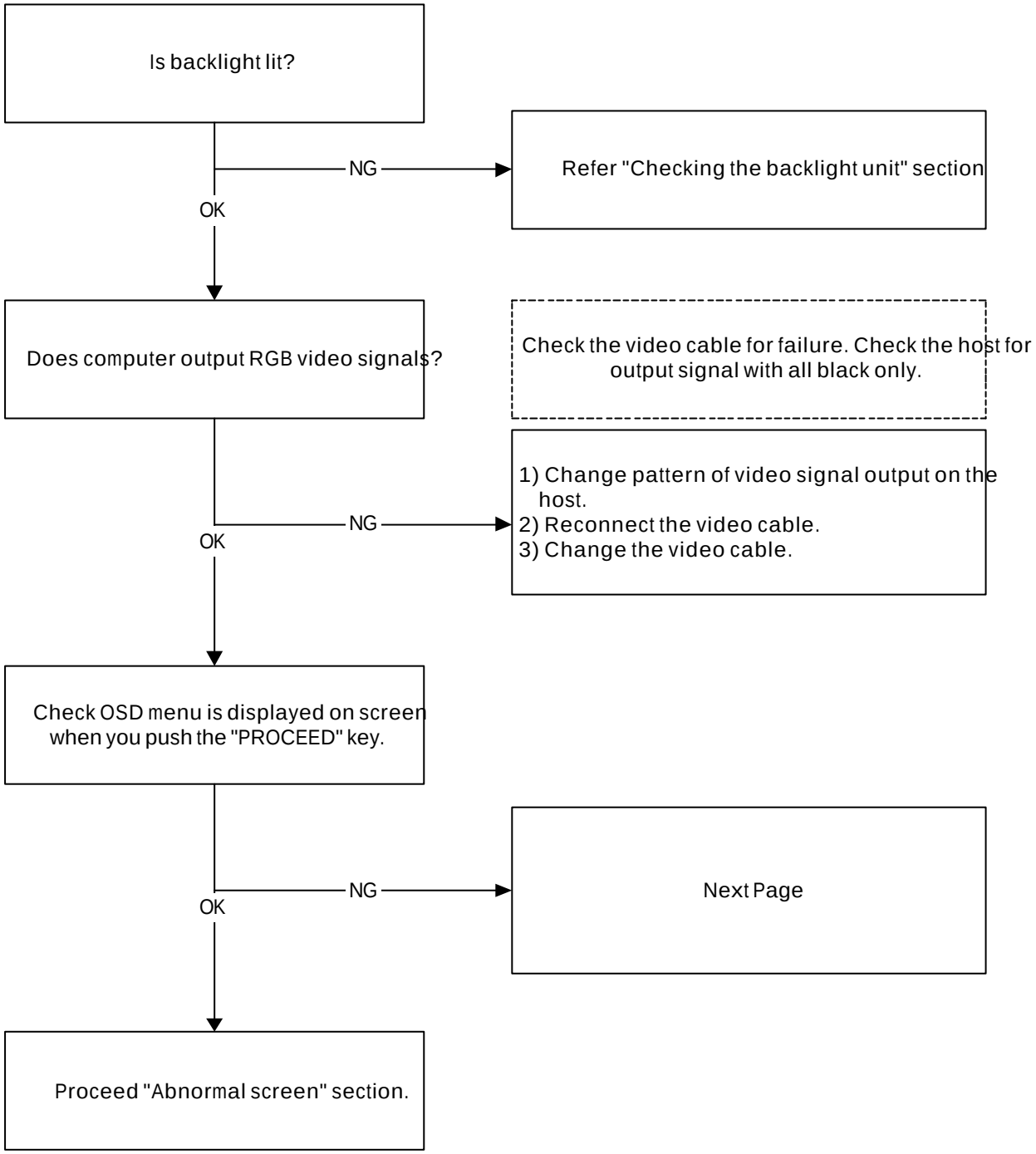
Inverter Board Block Diagram

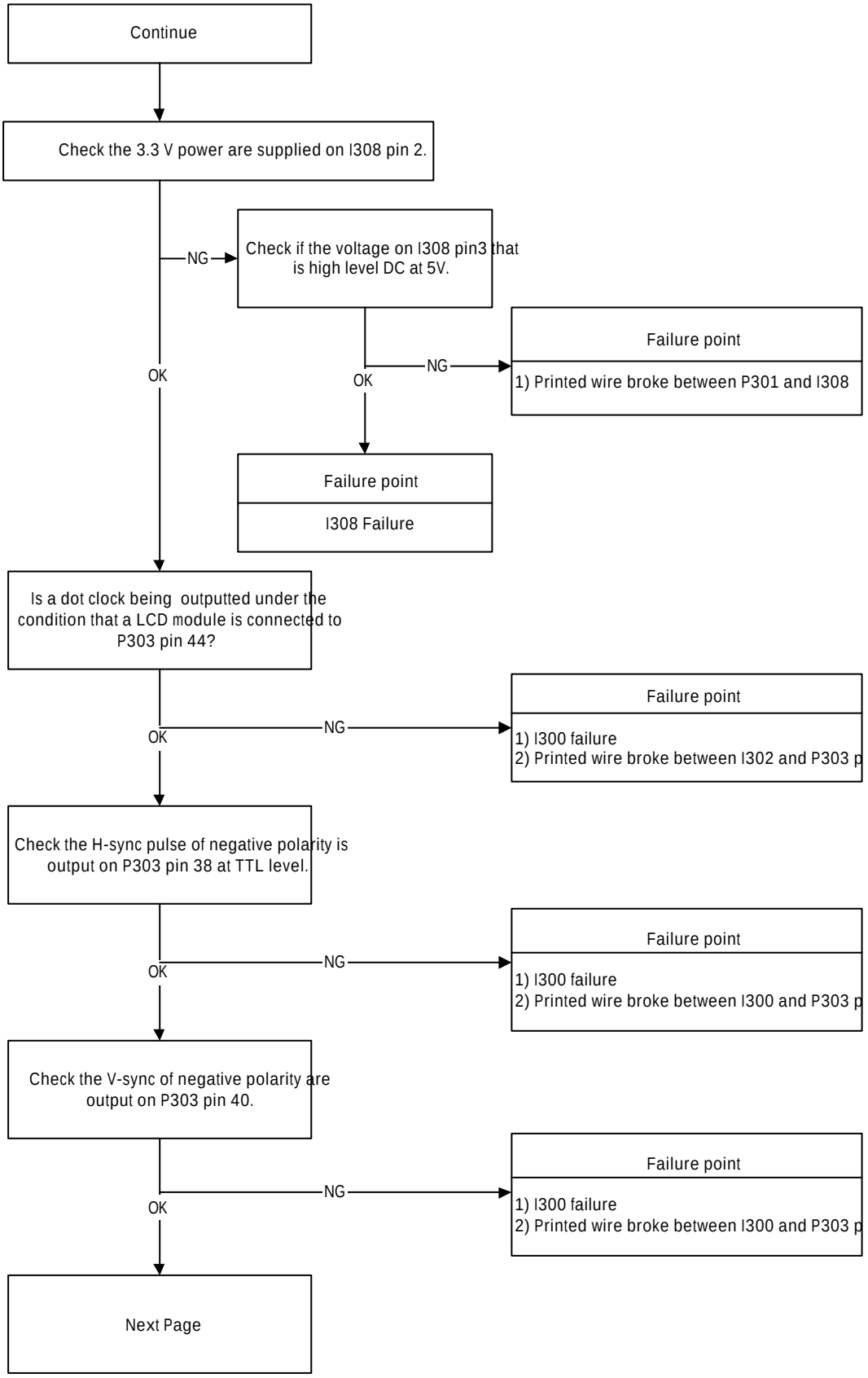


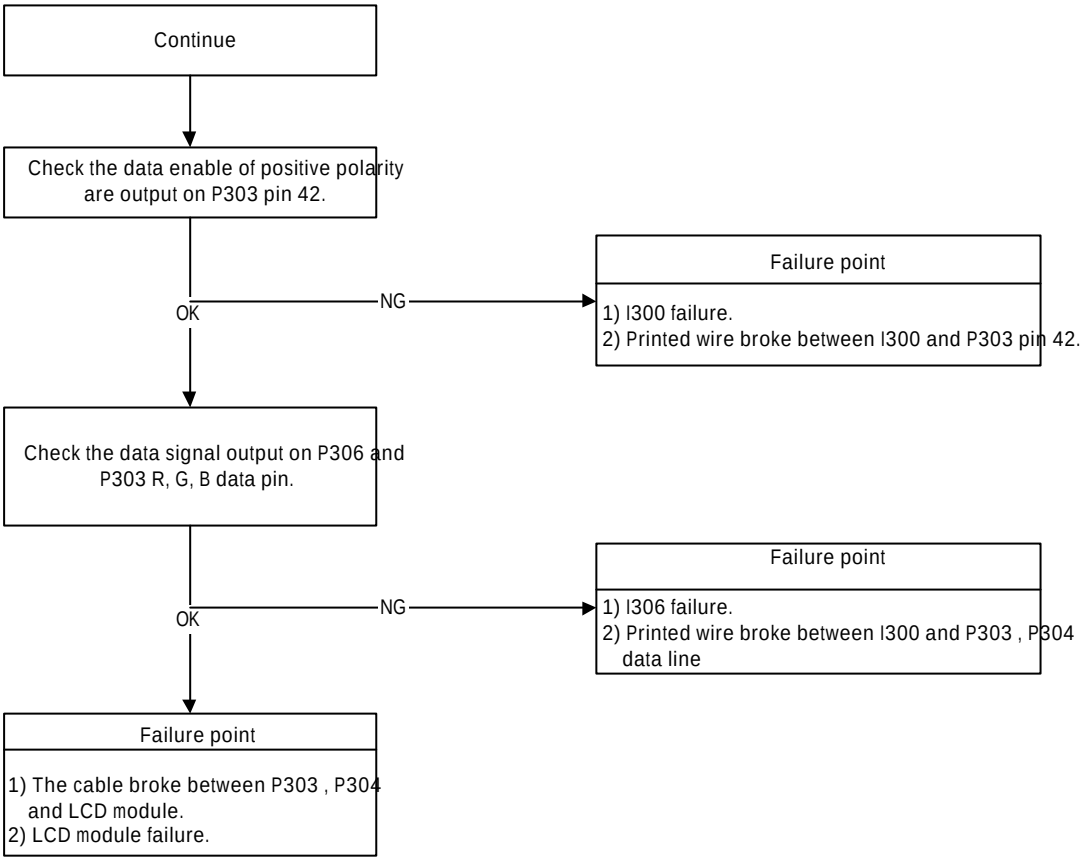
1. No display of screen (Screen is black, color of LED is amber)



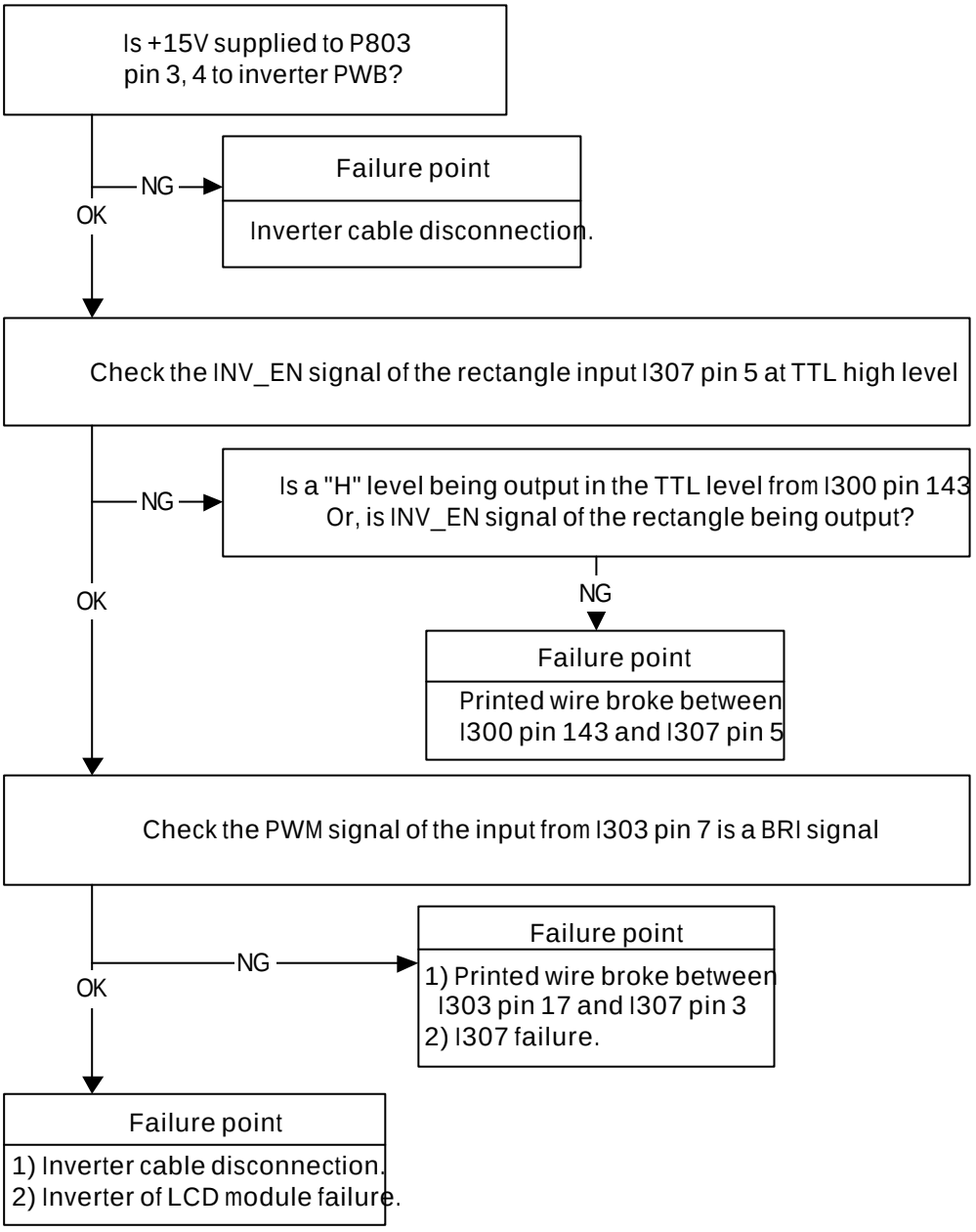
2. Nothing displays on screen (Screen is black, color of LED is green)



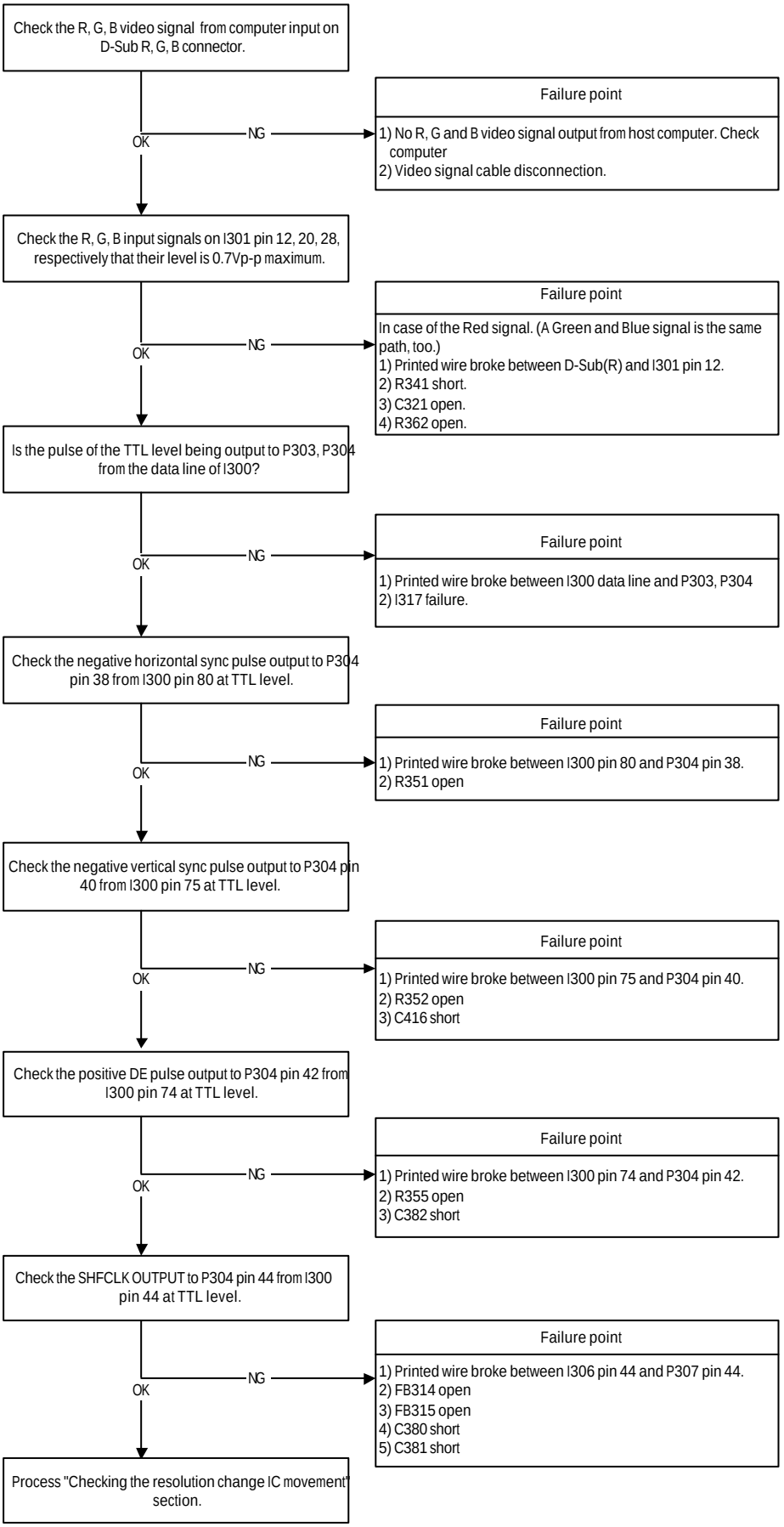

Continue
Check the 3.3 V power are supplied on I308 pin 2.
NG
Check if the voltage on I308 pin3 that is high level DC at 5V.
OK
NG
OK
Failure point
1) Printed wire broke between P301 and I308
Failure point
I308 Failure
Is a dot clock being outputted under the condition that a LCD module is connected to P303 pin 44?
OK
NG
Failure point
1) I300 failure
2) Printed wire broke between I302 and P303 p
Check the H-sync pulse of negative polarity is output on P303 pin 38 at TTL level.
OK
NG
Failure point
1) I300 failure
2) Printed wire broke between I300 and P303 p
Check the V-sync of negative polarity are output on P303 pin 40.
OK
NG
Failure point
1) I300 failure
2) Printed wire broke between I300 and P303 p
Next Page


Continue
Check the data enable of positive polarity are output on P303 pin 42.
NG
OK
Failure point
1) I300 failure.
2) Printed wire broke between I300 and P303 pin 42.
Check the data signal output on P306 and P303 R, G, B data pin.
NG
OK
Failure point
1) I306 failure.
2) Printed wire broke between I300 and P303 , P304 data line
Failure point
1) The cable broke between P303 , P304 and LCD module.
2) LCD module failure.

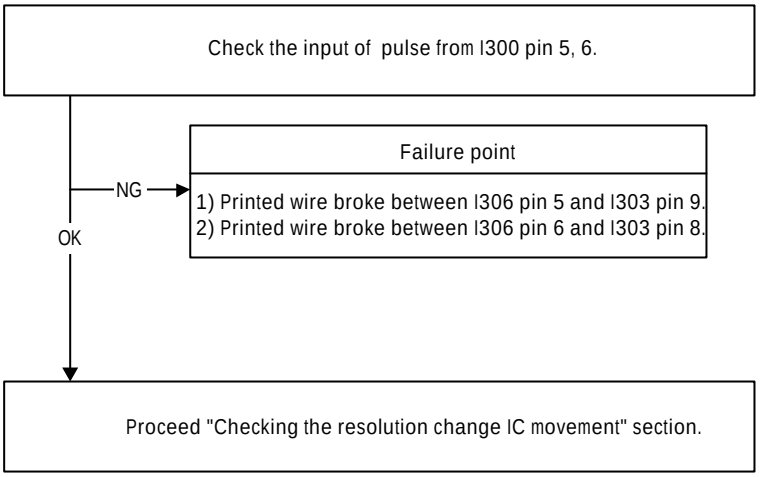
3. Checking the back light unit



4. Abnormal screen

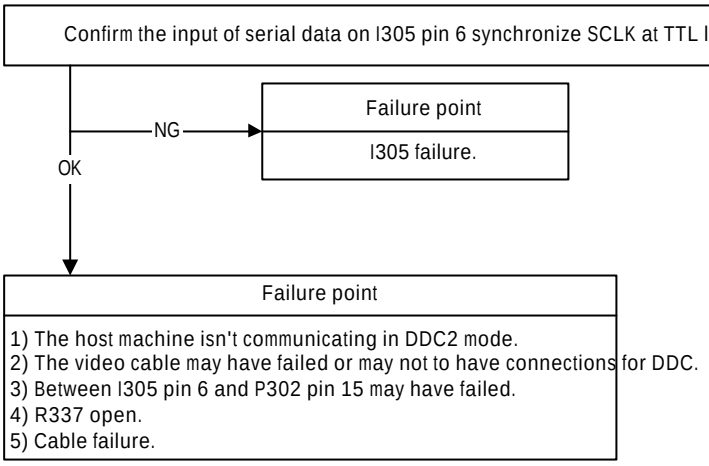


5. NO OSD display



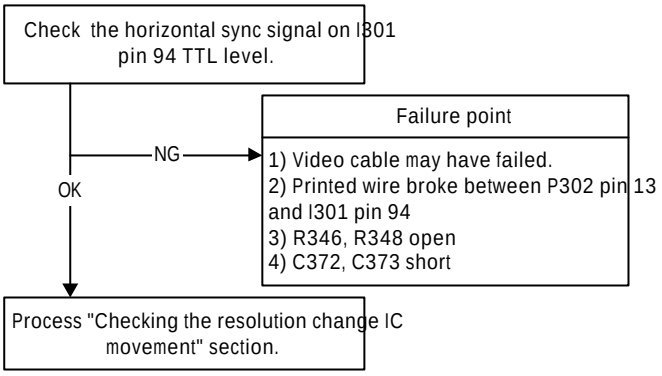
6. Abnormal plug and play operation

6.1 Abnormal DDC2

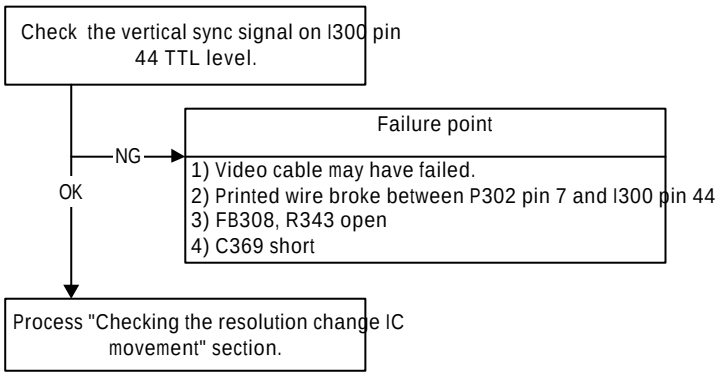


7. Checking the interface circuit of sync signal

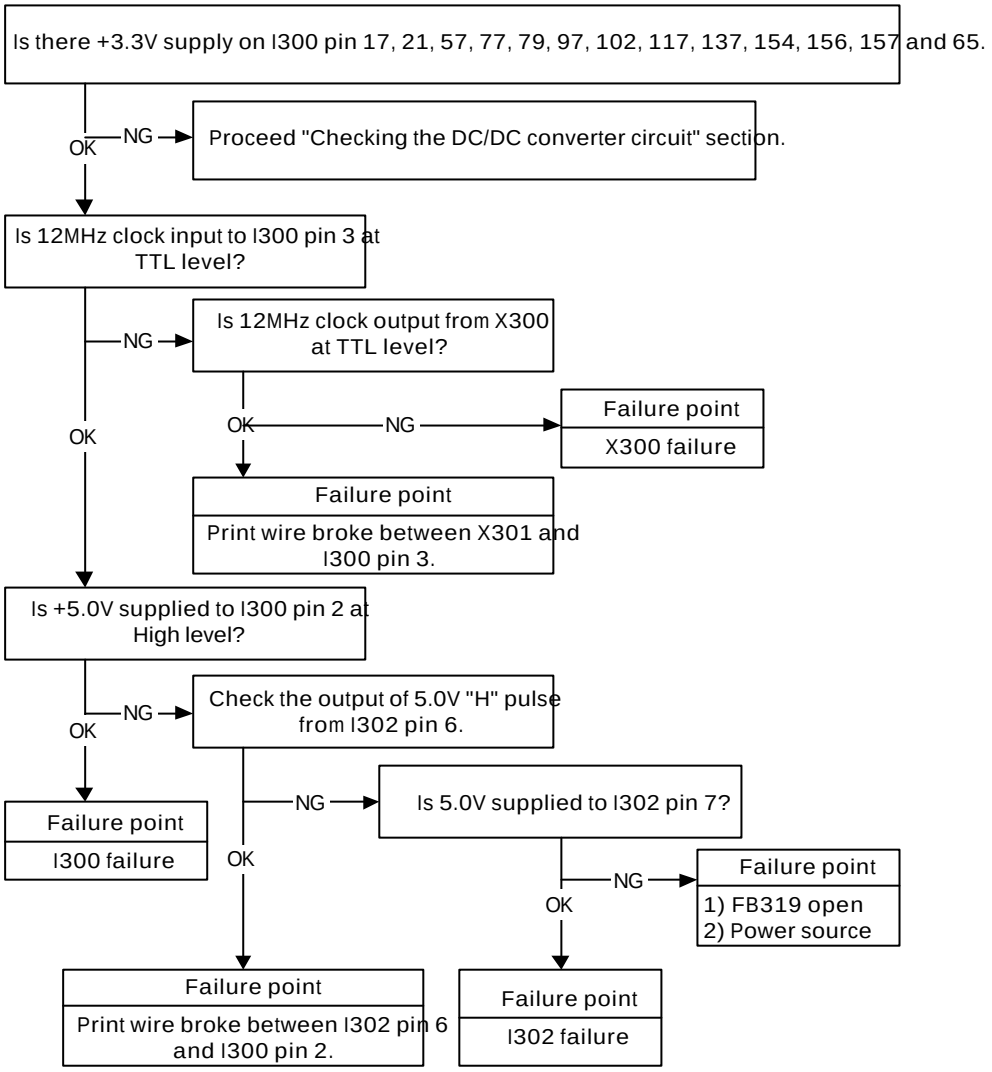
7.1 Checking the control circuit of horizontal sync pulse



7.2 Checking the control circuit of vertical sync pulse

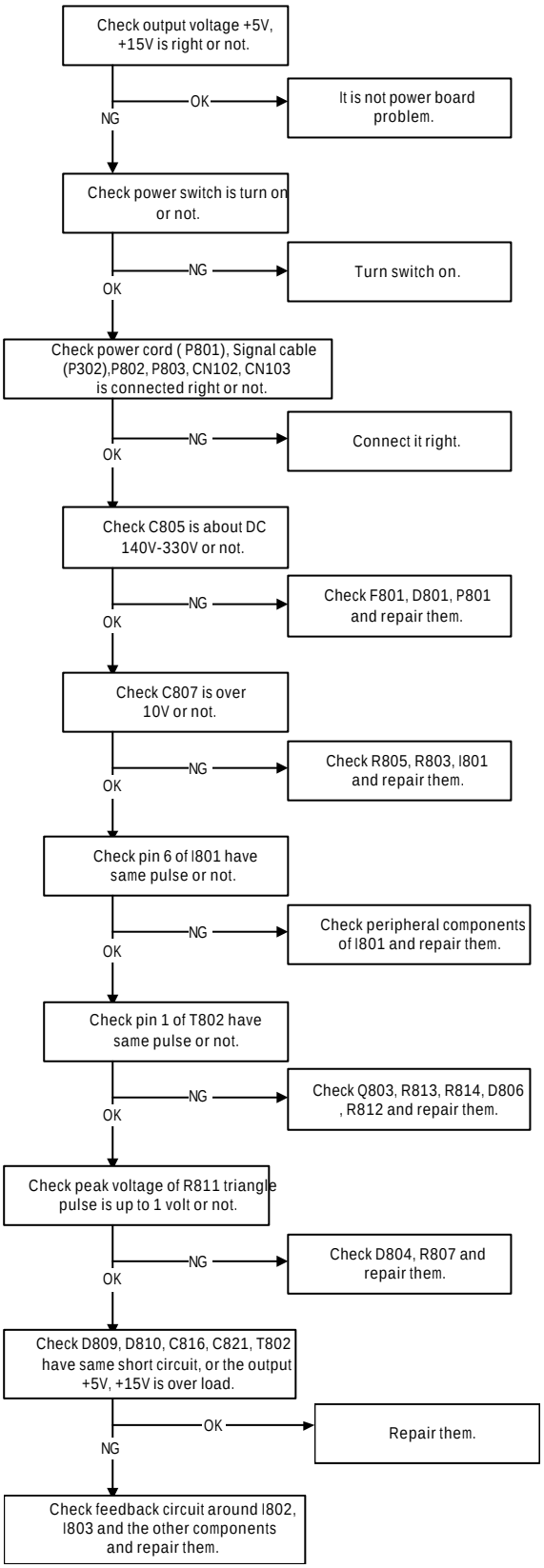


8. Checking the resolution change IC movement

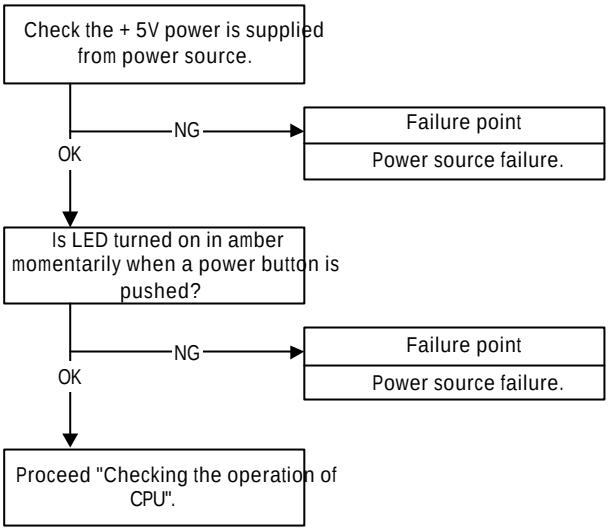


9. No power on

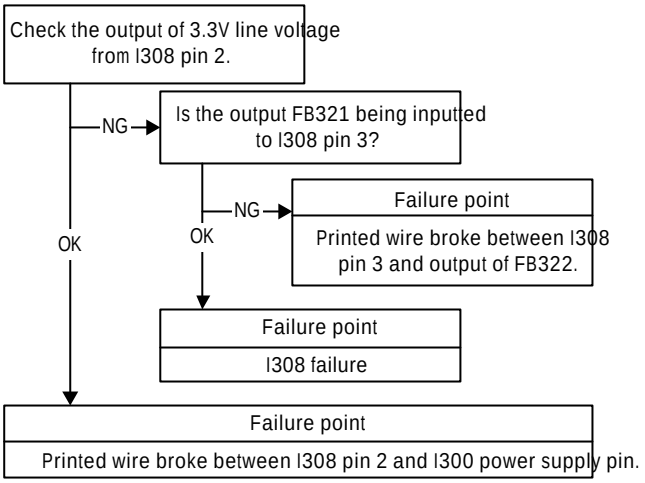
9.1 No power on (I)



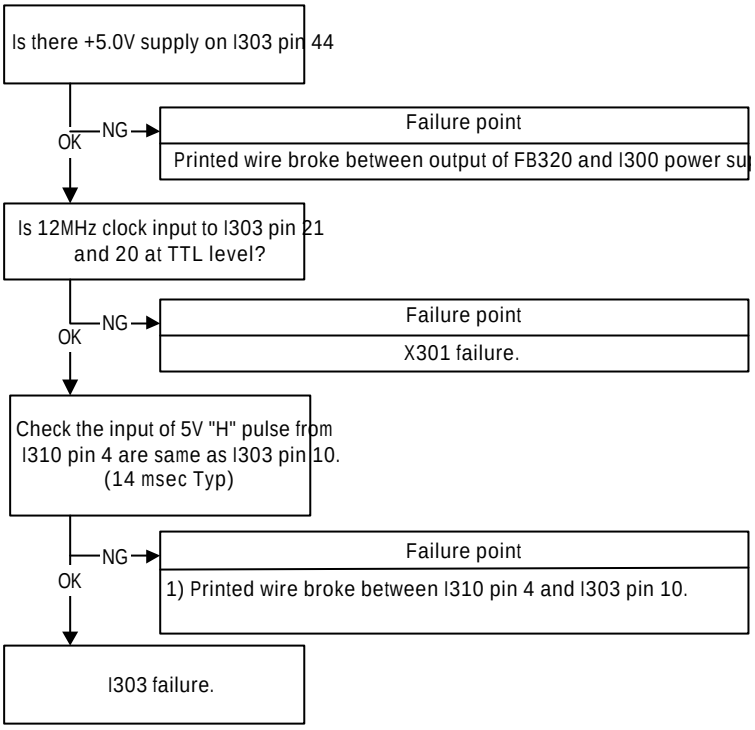
9.2 No power on (II)



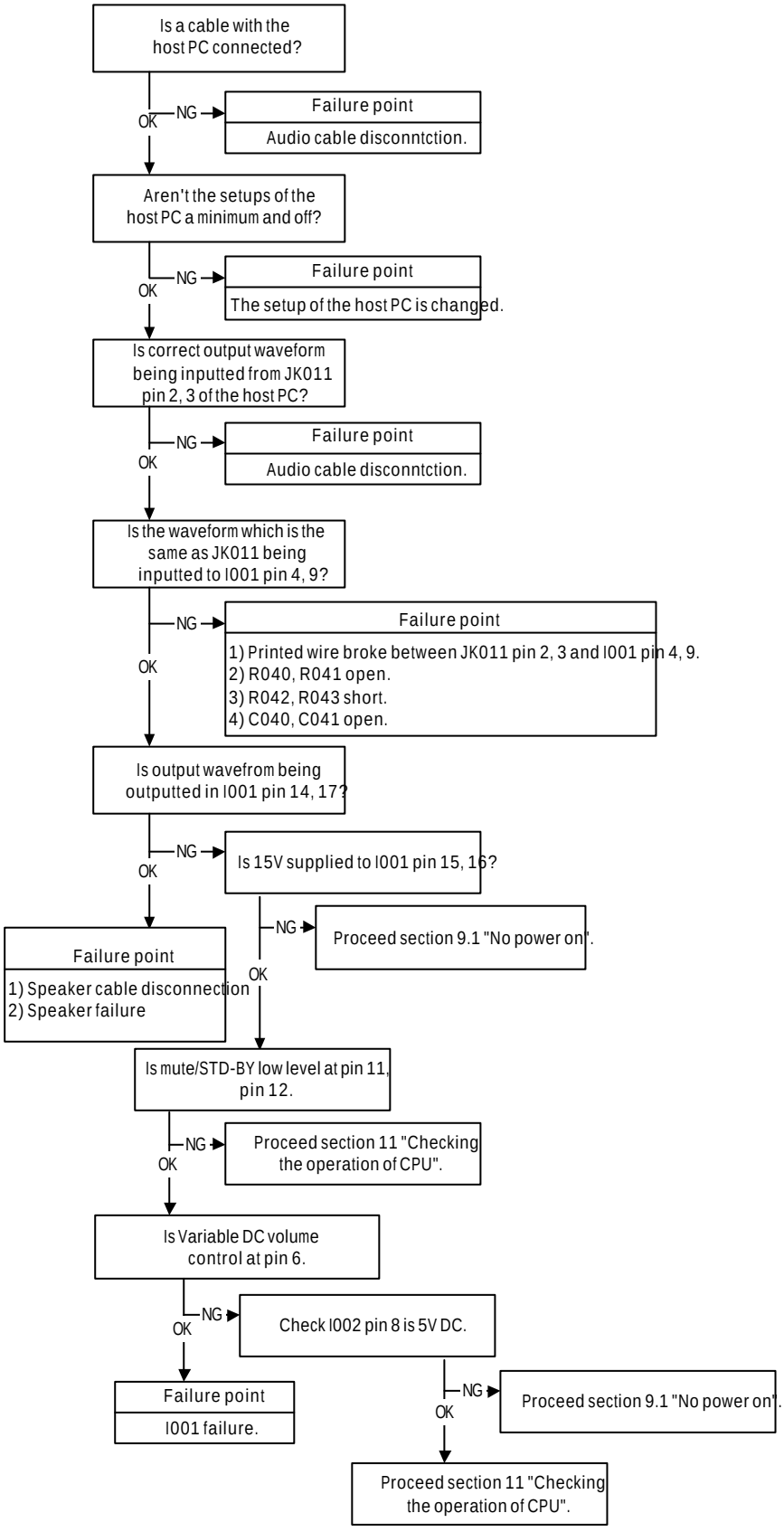
10. Checking the DC/DC converter circuit



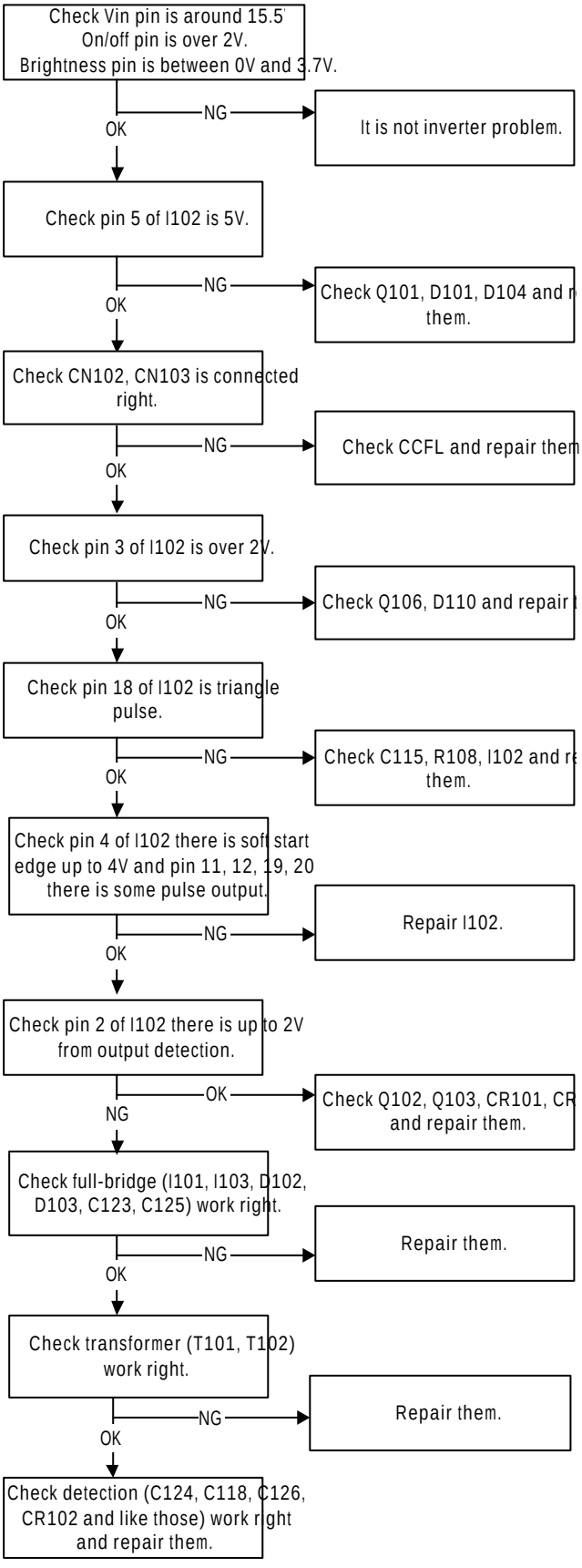
11. Checking the operation of CPU



12. Checking the audio circuit



13. Checking inverter board circuit



1. Recommended Parts List

Note: 1. The components identified by " ⚠ " mark are critical for X-ray safety. Replace these with only the same parts specified.

2. The components identified by " * " mark are critical parts.

3. There is only OTP IC at the model beginning (FPR stage or before). When it put in mass production and there must be Mask coming out. Please checkyou have spart parts need, please check BOM to get the last release part number and related information.

No.	Location	Part Number	Description
1 ***	I300	6447000406	IC MASCOT II CONTROLLER 160P PQFP
2 *	I301	6447000506	IC VITESSEI 100P QFP
3 *	I310	6446008108	IC NC7SZ04M5X SOT-23-5
4 **	I304	6448016508	IC EEPROM-24LC16B/SN SOP-8
5 **	I301	6447000506	IC ASIC-VITESSE2-100P-QFP
6 **	I307	6442001978	IC LM358DR 8P SOP
7 *	I308	6442023326	IC AIC1084-33CM 3P T0263
8 ***	Q300	6442007208	TR NPN SST2222A SOT-23
9 **	Q302	6427002508	FET-P-CHNL SI2305D3 SOT-2-3
10 ***	Q303	6442007308	TR NPN SST3904 SOT-23
11 ***	I001	6442023100	IC LINEAR-TDA7496L PDIP
12 *	I303	6448018900	IC CPU SM89516C25J PLCC44P